

MSH: A Multi-Stage HiZ-Aware Homotopy Framework for Nonlinear DC Analysis

Zhou Jin¹, Tian Feng², Xiao Wu², Dan Niu³, Zhenya Zhou² and Cheng Zhuo⁴

1. Super Scientific Software Laboratory, China University of Petroleum-Beijing, Beijing, China

2. Huada Emperean Software Co. Ltd, Beijing, China

3. School of Automation, Southeast University, Nanjing, China

4. College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China

Emails: jinzhou@cup.edu.cn, {fengtian, wuxiao, zhouzhy}@emperean.com.cn, danniu2013@seu.edu.cn, czhuo@zju.edu.cn

Abstract—Nonlinear DC analysis is one of the most important tasks in transistor-level circuit simulation. Homotopy gains great success to eliminate non-convergence problem occurred in the Newton-Raphson (NR) based methods. However, nonlinear circuits with DC-path available high impedance (HiZ) nodes may fail to converge with homotopy methods due to sufficiently large resistance compared to homotopy insertions, leading to an insufficiently close enough initial-guess. In this paper, we propose a HiZ-aware homotopy framework, MSH, enabling multi-stage continuation for HiZ nodes and others separately to enhance simulation convergence. In addition, a brand-new homotopy function with limited current gain variation for MOS transistors is utilized to ensure smoother solution curve and better efficiency. Moreover, we trace the solution curve with arclength by considering homotopy parameters as unknown variables to better ensure convergence. The effectiveness of our proposed homotopy framework is demonstrated on large-scale industrial-level circuits.

Index Terms—Circuit simulation, DC analysis, homotopy method, nonlinear CMOS circuit, high impedance node.

I. INTRODUCTION

The convergence of nonlinear DC analysis has always been a great challenge in back-end circuit simulation and verification [1]. DC analysis, to compute DC operating points, requires to solve a series of nonlinear algebraic equations established from the modified nodal analysis, where the Newton-Raphson (NR) is the most classic approach to be employed [2]–[4]. However, its convergence highly depends on the given initial guess. Due to the strong nonlinearity of analog circuits, it is highly difficult to provide a good initial guess that is sufficiently close to the real solution for the standard NR approach and its variants (as shown in Fig.1(a)) [5].

To address this issue, far more robust homotopies have been proposed from different perspectives in recent years [6]–[11]. Homotopy methods leverage a continuous mapping strategy from the viewpoint of mathematics transforming original hard-to-solve equations into equations with known solutions or that are easy to solve. Then, with homotopy parameter λ changes from 0 to 1, we can gradually iterate back to the original circuit, whose solution can be considered as a good initial solution for NR iteration. A positive example of the application of homotopy is shown in Fig. 1(b), which is a Schmitt Trigger circuit. The homotopy approaches are proven invariably convergence with probability-one theoretically. Reality has also proven that

homotopy methods do offer a feasible avenue for settling the matter of NR non-convergence [7], [8].

However, a new group of non-convergence situations has been found in the actual simulation of industrial-level large-scale complex circuit. Even though homotopy converges successfully, the homotopy convergent solution cannot be used as a good initial solution for NR iteration. For such circuits, the DC analysis will eventually fail to converge. In fact, such convergence failure is mainly caused by certain DC-path available HiZ nodes, whose node voltages will influence the circuit behaviour. With the homotopy parameter embedded, the voltages at such nodes are pushed to zero leading to a faraway initial guess for NR.

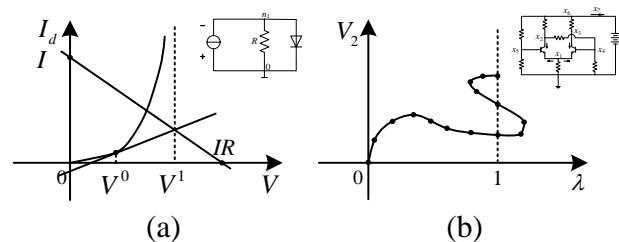


Fig. 1. (a) NR fails to converged due to numerical overflow; (b) homotopy method converges easily.

In this paper, we propose an effective multi-stage homotopy framework to resolve this problem, which can first iterate the HiZ nodes to DC solutions and then solve the DC solutions of non-HiZ nodes. We highlight the contributions of this work as follows:

- This paper proposes a multi-parameter homotopy framework enabling multi-stage continuation to resolve convergence failure caused by certain HiZ nodes in nonlinear DC analysis.
- The framework is equipped with a brand-new homotopy function to achieve fast continuation and adopts arclength method for tracing solution curves to ensure convergence.
- The proposed framework has been implemented and integrated in a SPICE-like simulator and is verified by industrial-level large-scale complex designs. Non-convergence issues are well resolved demonstrating its effectiveness. Moreover, it achieves an average 1.7x speed-up over SOTA fixed-point homotopy.

II. BACKGROUND

A. Problem Definition

The problem of computing DC operating points is equivalent to find the solution of a series of nonlinear algebraic equations established by the modified nodal analysis (MNA) method [11]. The nonlinear system describes the DC behavior of the electronic circuits and can be represented as follows,

$$\mathbf{F}(\mathbf{x}) = 0, \mathbf{x} \in \mathbb{R}^n, \mathbf{F}(\mathbf{x}) \in \mathbb{R}^n \rightarrow \mathbb{R}^n, \quad (1)$$

where \mathbf{x} is the unknown vector of node voltages and internal currents of the independent voltage sources, and n is the number of unknowns.

B. Homotopy Method

The fundamental idea of homotopy is to parameterize the nonlinear system shown in Eq. (1). Formally, a scalar parameter $\lambda \in [0, 1]$ is embedded into $\mathbf{F}(\mathbf{x})$ and the new equation can be written as

$$\mathbf{H}(\mathbf{x}, \lambda) = 0, \quad (2)$$

where $\mathbf{H}(\mathbf{x}, \lambda) \in \mathbb{R}^n \times \mathbb{R} \rightarrow \mathbb{R}^n$. For $\lambda = 0$, $\mathbf{H}(\mathbf{x}, 0) = 0$ is an equation that is easy to solve. For $\lambda = 1$, $\mathbf{H}(\mathbf{x}, 1) = 0$ is the original problem shown in Eq. (1).

Many homotopy methods with various auxiliary operators have been researched. Newton homotopy (NH) [6] is one of the most useful approaches for solving nonlinear BJT circuits. However, the globally convergent property of NH is bound by the uniform passivity of the initial point. Nonlinear homotopy (NLH) [10] is proposed for MOS circuits. Though it further extends the homotopies used for MOS circuits, the high demand of computing has restricted its efficiency. Furthermore, the inserted equivalent devices of NH and NLH usually include diodes that are quite complex to implement. The variable gain homotopy (VGH) [7], [9] and the variable gain Newton homotopy (VGNH) [12] are two efficient approaches for smoothing solution curve. However, they are mainly designed for BJT circuits. Few researches have considered MOS circuits. And unfortunately, for these homotopy methods, the implementation of equivalent circuit that guarantees the global convergence of the homotopy function is extremely complicated, prohibiting their widespread application in real industrial circuit simulators. The fixed-point homotopy (FPH) is considered as the most practical alternative [13] owing to the ease of realization and satisfactory convergence performance and efficiency. It is based on the equation

$$\mathbf{H}(\mathbf{x}, \lambda) = \lambda \mathbf{F}(\mathbf{x}) + (1 - \lambda) \mathbf{G}(\mathbf{x} - \mathbf{a}), \quad (3)$$

where \mathbf{G} is a $n \times n$ nonsingular matrix and \mathbf{a} is the initial guess vector.

C. Arclength Method

Many practical problems may occur when we trace the solution curve of the homotopy equation (2), especially in nonlinear circuits. One of the most common problems during the curve tracing process is that the curve folds back [14]. At the sharp turning point, the value of λ would decrease as the

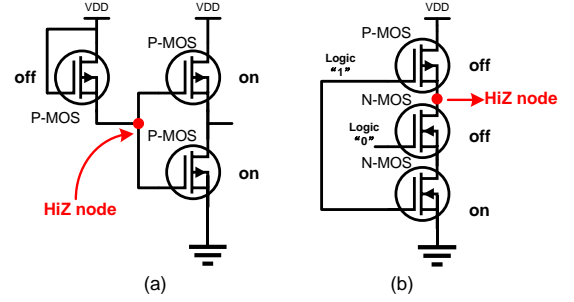


Fig. 2. (a) Floating HiZ node: a VDD-connected P-MOS gate causing a floating node [16]. (b) HiZ node with DC path: the node between two MOSFET transistors in “off” state, which is caused by their gate voltages.

path moves forward. If we continue to increase λ from 0 to 1 at this time point, we will lose the curve.

Arclength method [15] is regarded as an effective way for overcoming this difficulty. It considers λ as a function of the arc length s , where s satisfies

$$\sum_{i=1}^m \left(\frac{dx_i}{ds}\right)^2 + \left(\frac{d\lambda}{ds}\right)^2 = 1. \quad (4)$$

And then, the final solutions can be obtained by combining Eq. (2) and Eq. (4).

D. HiZ Nodes

HiZ state is a common output state of the circuit, which usually indicates that a node in the circuit has a higher impedance relative to other nodes in the circuit. Actually, the existence of HiZ nodes in circuit simulation can typically be divided into two types. The first one is the floating HiZ node created by connectivity problems in the design, such as a VDD-connected P-MOS gate displayed in Fig. 2(a). The second one is the HiZ node with DC-path like Fig. 2(b), which is determined by the stimuli. In contrast to the floating HiZ node, the latter controls other components in the circuit and therefore reflects more influence from DC algorithms.

III. PROPOSED METHOD

In this section, we first elaborate on the convergence failure of the homotopy method caused by certain HiZ nodes in DC analysis through an example demonstrated in Section III-A. Then in Section III-B, a general multi-stage homotopy framework is proposed for addressing this problem, which has three main innovation points. Finally, a simple HiZ nodes locating algorithm is introduced in Section III-C.

A. HiZ-Caused Failure in DC Analysis

As shown in Fig. 3(a), three P-MOS transistors $M1$, $M2$, and $M3$ are connected to each other through three small linear resistors less than $10^2 \Omega$. The source of $M1$ is connected to VDD, the drain of $M2$ is connected to VSS, and the gate of $M3$ is connected to $R2$ and $R3$. For DC analysis, when the gate voltages of $M1$ and $M2$ change to logic high, $M1$ and $M2$ will be in an off state. Meanwhile, $M3$ is disconnected throughout the DC analysis because only its gate is connected

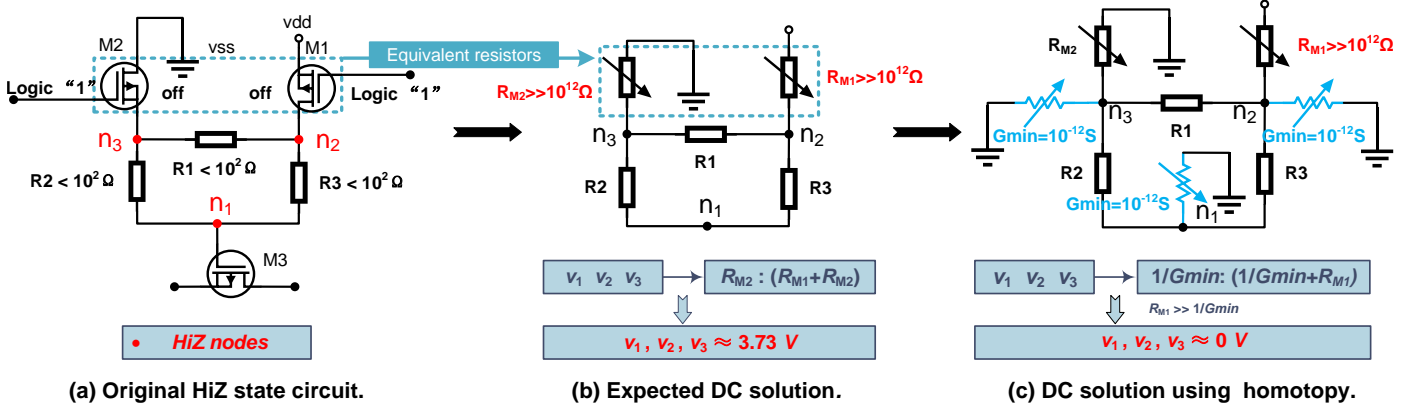


Fig. 3. Illustration of the convergence failure caused by HiZ nodes in DC homotopy algorithms. (a) This is a toy circuit including three HiZ nodes with DC path whose node voltages will control the state of $M3$. (b) The MOS transistors $M1$ and $M2$ in "off" state can be equivalent two infinite resistances R_{M1} and R_{M2} . Then the voltages at these HiZ nodes are supposed to be dominant by Eq. (5) ~ (7), e.g., in this case, $v_1 = v_2 = v_3 \approx 3.73V$. (c) Solving this circuit with homotopy algorithm, e.g. grounding each node with a $Gmin$, faces a fatal non-convergence problem. The reason is that though the homotopy continuation can successfully converge, the solution obtained in fact is far away from real solution. In this case, the solution is mainly determined by the Eq. (9) ~ (11). Though $Gmin$ is sufficiently small that satisfies the convergence tolerance, e.g. $1e-12$, we still have $R_{M1} \gg \frac{1}{Gmin}$, making $v_1 = v_2 = v_3 \approx 0V$. This result raises convergence failure at final NR verification stage.

to the circuit. Hence the three nodes $n_1 \sim n_3$ are in a HiZ state. At the moment, we can regard $M1$ and $M2$ as two infinite resistances R_{M1} and R_{M2} ($\gg 10^{12}\Omega$) as shown in Fig. 3(b). Since $R1, R2$ and $R3$ are small enough compared to R_{M1} and R_{M2} , the DC solutions of these three HiZ nodes (i.e. v_1, v_2, v_3) are supposed to be determined by the following formula (5), (6), (7):

$$v_1 = \frac{R2}{R2 + R3} \cdot (v_2 - v_3) + v_3 \approx \frac{R_{M2} \cdot VDD}{R_{M1} + R_{M2}}, \quad (5)$$

$$v_2 = \frac{R_{M2} + \frac{R1(R2+R3)}{R1+R2+R3}}{R_{M1} + R_{M2} + \frac{R1(R2+R3)}{R1+R2+R3}} \cdot VDD \approx \frac{R_{M2} \cdot VDD}{R_{M1} + R_{M2}}, \quad (6)$$

$$v_3 = \frac{R_{M2}}{R_{M1} + R_{M2} + \frac{R1(R2+R3)}{R1+R2+R3}} \cdot VDD \approx \frac{R_{M2} \cdot VDD}{R_{M1} + R_{M2}}. \quad (7)$$

Note that the ratio of R_{M2} to $(R_{M1} + R_{M2})$ is a certain number even though they both are sufficiently large. In this case, the result is $v_1 = v_2 = v_3 \approx 3.73V$, which is the expected DC solutions.

However, if we solve the DC solution by homotopy method, such as grounding each node with a $Gmin$ as shown in Fig. 3(c), the solution we obtained would be far away from the real solution leading to a failure DC analysis. Generally, we consider the solution to be the initial value of final NR verification when the value of $Gmin$ decreases from 1 to a very small value (e.g. $10^{-12}S$). At this moment, three HiZ node voltages are evaluated by formula (9), (10), (11), where R_t is the total resistance of this circuit.

$$R_t \approx R_{M1} + \frac{1}{Gmin}. \quad (8)$$

$$v_1 = v_2 - \left[\frac{\frac{R3/Gmin}{R3+1/Gmin}}{\frac{R3/Gmin}{R3+1/Gmin} + \frac{R2/Gmin}{R2+1/Gmin}} \right] \cdot (v_2 - v_3) \quad (9)$$

$$\approx \frac{VDD/Gmin}{R_{M1} + 1/Gmin}.$$

$$v_2 = \left[\frac{R1 \left(\frac{R3/Gmin}{R3+1/Gmin} + \frac{R2/Gmin}{R2+1/Gmin} \right)}{\frac{R3/Gmin}{R3+1/Gmin} + \frac{R2/Gmin}{R2+1/Gmin} + R1} + \frac{R_{M2}}{R_{M2} + \frac{1}{Gmin}} \right] \cdot \frac{VDD}{R_t} \approx \frac{VDD/Gmin}{R_{M1} + 1/Gmin}. \quad (10)$$

$$v_3 = \left(\frac{R_{M2}/Gmin}{R_{M2} + 1/Gmin} \right) \cdot \frac{VDD}{R_t} \approx \frac{VDD/Gmin}{R_{M1} + 1/Gmin}. \quad (11)$$

The fact that $R_{M1} (\gg 10^{12}\Omega)$ usually far outweigh $\frac{1}{Gmin}$ ($\approx 10^{12}\Omega$) makes $v_1 = v_2 = v_3 \approx 0$, which would raise convergence failure at final NR verification stage.

B. A General Multi-Stage Homotopy Framework

This part will introduce our proposed multi-stage homotopy framework from three aspects: algorithm framework, construction of homotopy function and tracing solution curve. As a supplement, we will also briefly introduce the final NR verification.

1) Multi-stage and multi-parameter homotopy framework:

Unlike a conventional homotopy that all node voltages are solved simultaneously, our framework employs a hybrid of both multi-stage and multi-parameter to enable HiZ nodes and non-HiZ nodes to be solved separately, prohibiting the occurrence of non-convergence at final NR verification. The brand-new homotopy function is defined as follows:

$$\mathbf{H}(\mathbf{x}, \lambda_1, \lambda_2) = \begin{cases} \mathbf{h}(\mathbf{x}, \lambda_1) \\ \mathbf{h}(\mathbf{x}, \lambda_2) \end{cases}, \quad (12)$$

equations, where \mathbf{A} and \mathbf{A}' are two diagonal matrices, and $\mathbf{J}(\mathbf{x})$ is the Jacobi matrix of $\mathbf{F}(\mathbf{x})$.

$$\begin{bmatrix} \mathbf{J}(\mathbf{x}) - (1 - \lambda_1)\mathbf{g}'(\tilde{\mathbf{x}}_p) + \mathbf{A} & \mathbf{g}(\tilde{\mathbf{x}}_p) + \mathbf{A}' \cdot \mathbf{x} \\ (\mathbf{v}_x^p)^T & v_{\lambda_1}^p \end{bmatrix} \begin{bmatrix} \mathbf{v}_x \\ v_{\lambda_1} \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ 1 \end{bmatrix} \quad (18)$$

In the corrector step, the NR iteration can be written as:

$$\begin{bmatrix} \mathbf{J}(\mathbf{x}) - (1 - \lambda_1)\mathbf{g}'(\tilde{\mathbf{x}}_p) + \mathbf{A} & \mathbf{g}(\tilde{\mathbf{x}}_p) + \mathbf{A}' \cdot \mathbf{x} \\ \mathbf{v}_x^T & v_{\lambda_1} \end{bmatrix} \begin{bmatrix} d\mathbf{x} \\ d\lambda_1 \end{bmatrix} = \begin{bmatrix} -\mathbf{F}(\mathbf{x}) + (1 - \lambda_1)\mathbf{g}(\tilde{\mathbf{x}}_p) - \mathbf{A} \cdot \mathbf{x} \\ -\mathbf{v}_x^T(\mathbf{x} - \tilde{\mathbf{x}}^{k+1}) - v_{\lambda_1}(\lambda_1 - \tilde{\lambda}_1^{k+1}) \end{bmatrix}. \quad (19)$$

Note that, in order to avoid enlarging the matrix size when solving Eq. (18) and Eq. (19), we adopt the strategy used in the work of arclength method [11].

4) *NR evaluation at final stage*: After the homotopy solution is obtained through previous continuation, it is given as the initial guess for final stage NR evaluation. Generally, when homotopy parameter is sufficiently close to 1, that is, when $f_{abs}(\lambda - 1) < tol$ (tol is a given convergence accuracy) is satisfied, we hold the solution at this point as the DC solution. But strictly speaking, a circuit that satisfies the above convergence criterion may not equivalent to the original circuit, thus the above convergent solution cannot be directly used as the final DC solution. A more correct way is supposed to completely eliminate the homotopy operator embedded in the MNA equations and take the final convergent solution of homotopy as the initial value, then use NR to evaluate the true DC solution.

C. HiZ Nodes Location

To locate such HiZ nodes is also crucial. However, approaches that to locate accurately before simulation usually require high computational resources and do not bring a lot of benefits. Locate HiZ nodes after simple simulation could be much more easy and the non-convergence results could also indicate the problem. Instead of introducing additional overhead from detection approaches, here we introduce a simple yet effective technique for these DC path available HiZ nodes location. The detailed algorithm is shown in Algorithm 2. Considering simulation with normal DC algorithms for the circuit, if the non-convergence problem occurs while the right-hand-side is sufficiently close to 0, we firstly check the current of each non-convergent node. If the node current is less than the given threshold, a HiZ node is located.

IV. NUMERICAL EXAMPLES

In this section, our proposed multi-stage homotopy is applied to several large-scale MOS circuits from the real-world. Our approach is implemented in a C++ based SPICE-like circuit simulator. We would demonstrate the feasibility of our method from diverse perspectives. First, we illustrate the ability of our multi-stage framework to solve the HiZ state problem. After that, the convergence performance of MOS-relevant homotopy function is confirmed. Finally, the acceleration efficiency of our framework with MCGH is verified and compared with the framework using SOTA fixed-point homotopy approach [11]. The arclength method is used to trace the solution curves in all experiments.

Algorithm 2 Simple HiZ nodes detection strategy

```

1: Simulation with normal DC algorithm
2: if  $RHS \rightarrow 0$  and  $Terminate()$  does not converge then
3:   /*Check high-Z nodes*/
4:   for all non-convergent nodes do
5:     Calculate the current  $i_j (j = 1, \dots, m)$ 
6:     //  $m$  is the number of non-convergent nodes
7:     if  $i_j < i_{threshold}$  then
8:       Add node  $n_j$  into array  $highZ[]$ 
9:     end if
10:  end for
11: end if

```

A. Ability to Eliminate the HiZ Non-Convergence Problem

An industrial CMOS circuit is tested to verify our MSH framework, which consists of 69334 devices (including 715 MOS transistors). According to the experiment, totally 16 HiZ nodes are detected and the solution curve of one of them is shown in Fig. 5(a). For this circuit, we can discover that the SOTA homotopy approach can successfully converge, but fails to converge at the final NR stage. As expected, the circuit converges to its DC solution successfully at the final NR stage with our MSH framework. Detailed solution curve at the final stage ($\lambda \rightarrow 1$) is shown in Fig. 5(b). It can be observed that the final convergence voltage of SOTA homotopy is sufficiently close to zero as we demonstrated in Fig. 3, which is far away from the real DC solution. Also note that though our proposed framework needs two stage continuation, it will not introduce too much additional overhead since stage-I can usually reach their steady state easily with a small number of iterations.

B. Convergence Performance of MCGH

To make a better and fair performance demonstration of our proposed new continuation strategy for the MOS circuits from the standpoint of the model, here a large-scale circuit with 15884 devices (including 12765 MOS transistors) is also tested to verify its own convergence performance directly. Figure 6 displays the solution curves for the drain node of a MOSFET. For SOTA homotopy, the solution curve suffers from discontinuity when λ reaches around 0.96 due to the strong nonlinearity in current gains. Our MCGH can converge and the λ finally reaches 1. It can also be easily found that the nodal solution curve of our method is very smooth when λ is between 0 and 0.999. The large movement around $\lambda = 1$ is mainly due to the linear auxiliary item we introduced.

C. Acceleration Efficiency

Last, based on the convergence guaranteed by our MSH framework, we assess the acceleration efficiency of the MOS-relevant homotopy function. We test the MSH framework using MCGH function and SOTA fixed-point homotopy function respectively through several large industry MOS circuits, and record the number of NR iterations. Our proposed framework with MCGH demonstrates slightly superior acceleration, as evidenced by the results presented in Table I. Specifically, MCGH is able to reduce the number of NR iterations required to obtain

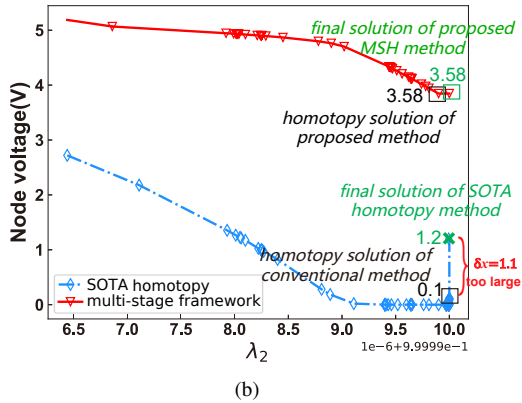
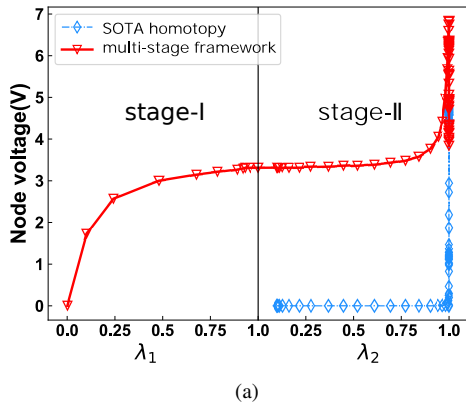


Fig. 5. (a) The solution curve of a HiZ node under two approaches. (b) Enlarged partial view when the λ_2 is very close to 1.

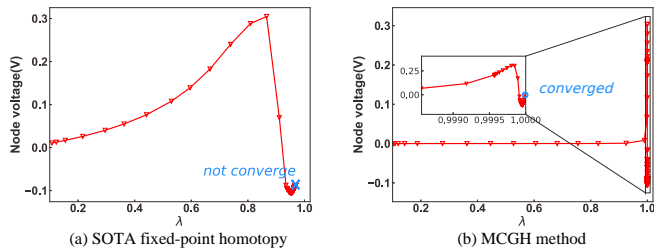


Fig. 6. The solution curve for the drain node of a MOSFET under two homotopy methods.

the DC solution, resulting in a relatively modest speedup of approximately 1.7x. This improvement can be attributed to the smoother solution curves that our method produces, which are able to converge to a solution more quickly and efficiently.

TABLE I
ACCELERATION OF OUR PROPOSED MCGH.

Circuits	r	c	didode	bjt	mos	#FPH ¹	#MCGH ²	Speedup
run300	1443601	1803000	0	0	360903	289	165	1.75
ss800u	1377	1746	3947	126	4954	141	89	1.58
steady	105056	3009	0	0	260450	270	161	1.68
mpq457	408	474	2530	50	2284	148	79	1.87

¹The number of NR iterations of fixed-point homotopy.

²The number of NR iterations of our proposed method.

V. CONCLUSION

In this paper, we propose a new multi-stage homotopy framework to resolve or avoid the non-convergence problem of existing DC algorithms caused by certain HiZ nodes. Remarkably, our framework is also equipped with an efficient

MOS homotopy function for fast continuation and robust arc-length approach for tracing solution curves. The effectiveness and efficiency are demonstrated by real-world industrial-level designs.

VI. ACKNOWLEDGMENTS

Dan Niu is the corresponding author of this paper. This work was supported by National Key R&D Program of China (Grant No. 2022YFB4400400), National Natural Science Foundation of China (Grant No. 62204265, 62234010), and Major Program of Zhejiang Provincial NSF(Grant No. D24F040002).

REFERENCES

- [1] Z. Jin, X. Wu, D. Niu, and Y. Inoue, "Effective implementation and embedding algorithms of cepta method for finding dc operating points," *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, vol. 96-A, pp. 2524–2532, 2013.
- [2] Z. Jin, M. Liu, and X. Wu, "An adaptive dynamic-element pta method for solving nonlinear dc operating point of transistor circuits," in *IEEE 61st International Midwest Symposium on Circuits and Systems*, 2018, pp. 37–40.
- [3] Z. Jin, X. Wu, D. Niu, X. Guan, and Y. Inoue, "Effective ramping algorithm and restart algorithm in the spice3 implementation for dpta method," *Nonlinear Theory and Its Applications, IEICE*, vol. 6, no. 4, pp. 499–511, 2015.
- [4] Z. Jin, H. Pei, Y. Dong, X. Jin, X. Wu, W. W. Xing, and D. Niu, "Accelerating nonlinear dc circuit simulation with reinforcement learning," in *Proceedings of the 59th ACM/IEEE Design Automation Conference*, ser. DAC '22, 2022, p. 619–624.
- [5] L. O. Chua, "Computer-aided analysis of electronic circuits," *Algorithms and computational techniques*, 1975.
- [6] A. Ushida, Y. Yamagami, Y. Nishio, I. Kinouchi, and Y. Inoue, "An efficient algorithm for finding multiple dc solutions based on the spice-oriented newton homotopy method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 337–348, 2002.
- [7] M. M. Green and R. C. Melville, "Sufficient conditions for finding multiple operating points of dc circuits using continuation methods," in *Proceedings of ISCAS'95-International Symposium on Circuits and Systems*, vol. 1. IEEE, 1995, pp. 117–120.
- [8] Y. Imai, K. Yamamura, and Y. Inoue, "An efficient homotopy method for finding dc operating points of nonlinear circuits," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 88, no. 10, pp. 2554–2561, 2005.
- [9] L. Trajkovic, R. C. Melville, and S.-C. Fang, "Finding dc operating points of transistor circuits using homotopy methods," in *1991., IEEE International Symposium on Circuits and Systems*. IEEE, 1991, pp. 758–761.
- [10] D. Niu, K. Sako, G. Hu, and Y. Inoue, "A globally convergent nonlinear homotopy method for mos transistor circuits," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 95, no. 12, pp. 2251–2260, 2012.
- [11] Z. Jin, T. Feng, Y. Duan, X. Wu, M. Cheng, Z. Zhou, and W. Liu, "Palbbd: A parallel arclength method using bordered block diagonal form for dc analysis," in *Proceedings of the 2021 on Great Lakes Symposium on VLSI*, 2021, pp. 327–332.
- [12] K. Yamamura and W. Kuroki, "An efficient and globally convergent homotopy method for finding dc operating points of nonlinear circuits," in *Proceedings of the 2006 Asia and South Pacific Design Automation Conference*, 2006, pp. 408–415.
- [13] C. Lemke, "Pathways to solutions, fixed points, and equilibria (cb garcia and wj zangwill)," 1984.
- [14] A. Ushida and L. Chua, "Tracing solution curves of non-linear equations with sharp turning points," *International journal of circuit theory and applications*, vol. 12, no. 1, pp. 1–21, 1984.
- [15] E. Ikeno and A. Ushida, "The arc-length method for the computation of characteristic curves," *IEEE Transactions on Circuits and Systems*, vol. 23, no. 3, pp. 181–183, 1976.
- [16] Z. Wang and H. Liu, "How to use virtuoso check/assertion flow in advanced node ic design," *Application of Electronic Technique*, vol. 82, no. 8, pp. 28–32, 2016.